US 20160276022A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2016/0276022 A1

(43) Pub. Date: Sep. 22, 2016

Redaelli

(54) CONSTRUCTIONS COMPRISING STACKED MEMORY ARRAYS

(71) Applicant: **Micron Technology, Inc.**, Boise, ID (US)

(72) Inventor: **Andrea Redaelli**, Casatenovo (IT)

(21) Appl. No.: **14/662,920**

(22) Filed: **Mar. 19, 2015**

Publication Classification

(51) **Int. Cl.**
G11C 13/00 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 13/0004*** (2013.01); ***G11C 13/003*** (2013.01)

(57) **ABSTRACT**

Some embodiments include a construction having a first memory array deck and a second memory array deck over the first memory array deck. The second memory array deck differs from the first memory array deck in one or more operating characteristics, in pitch, and/or in one or more structural parameters; with the structural parameters including different materials and/or different thicknesses of materials. Some embodiments include a construction having a first series and a third series of access/sense lines extending along a first direction, and a second series of access/sense lines between the first and third series and extending along a second direction which crosses the first direction. First memory cells are between the first and second series of access/sense lines and arranged in a first memory array deck. Second memory cells are between the second and third series of access/sense lines and arranged in a second memory array deck.